**Listing of Claims:**

Claim 1 (currently amended): In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a control processor comprising a means for ordering ~~user~~ the input signals; and

a plurality of SIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection and adaptive temporal reconstruction filtering in a successive arrangement wherein the output of one of ~~the~~ said processors is the input to ~~the~~ a next successive processor, each of said SIC-ATRF processors comprising:

a conventional detector;

a respread processor;

an adaptive temporal filter (ATRF); and

a complex mathematical operation processor for canceling ~~the~~ a reconstructed signal ~~for the user~~ from ~~the~~ a ~~total~~ received signal.

Claim 2 (original): The combination of claim 1 wherein each conventional detector is an IS-95 conventional detector comprising a short code despreader, a long code despreader, and a 64-ary matched filter bank.

Claim 3 (original): The combination of claim 1 wherein each conventional detector is an IS-95 rake conventional detector.

Claim 4 (original): The combination of claim 1 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

Claim 5 (original): The combination of claim 4 wherein each SIC-ATRF processor further comprises a minimum cost channel estimate (MCCE) weight update processor.

Claim 6 (original): The combination of claim 4 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

Claim 7 (original): The combination of claim 4 wherein each ATRF is a minimum mean square error filter.

Claim 8 (currently amended): The combination of claim 1 wherein the output of each respread processor is ~~the~~ an input for the ATRF.

Claim 9 (currently amended): The combination of claim 8 wherein the input to each ATRF further comprises ~~the~~ outputs of the respread processors in all ~~the~~ previous SIC-ATRF processors.

Claim 10 (original): The combination of claim 1 wherein each SIC-ATRF processor further comprises a frequency shift processor connected between the respread processor and the adaptive temporal filter.

Claim 11 (original): The combination of claim 10 wherein each frequency shift processor comprises means to shift the frequency of the signal output from the respread processor to take into account Doppler spread.

Claim 12 (currently amended): A method in a combination system for enabling ~~the~~ a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering ~~user~~ the input signals according to a pre-defined methodology and assigning each ~~user~~ input signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, an adaptive temporal ~~filter;~~ filter, and a complex mathematical operation processor for canceling ~~the~~ a reconstructed signal ~~for the user~~ from ~~the~~ a ~~total~~ received signal;

communicating a separate user code associated with ~~the user~~ an input signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired ~~user~~ input signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

estimating a channel for the ~~user~~ input signal associated with the SIC-ATRF processor and reconstructing ~~the~~ a signal interference associated with the ~~user~~ input signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the ~~user~~ input signal associated with the SIC-ATRF processor from the ~~total~~ received ~~signal.~~ signal to create an output; and

if a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to ~~the~~ a successive SIC-ATRF processor.

Claim 13 (currently amended): The method of claim 12 wherein the step of ordering ~~user~~ the input signals according to a pre-defined methodology comprises ranking signals in descending order of received powers.

Claim 14 (currently amended): The method of claim 12 wherein the step of ordering ~~user~~ the input signals according to a pre-defined methodology comprises identifying signals above a certain threshold.

Claim 15 (currently amended): The method of claim 12 wherein the channel estimation step further comprises:

determining ~~the~~ adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

Claim 16 (original): The method of claim 15 wherein the pre-determined cost function is a minimum mean square error function.

Claim 17 (currently amended): The method of claim 12 wherein the channel estimation step further comprises:

determining ~~the~~ adaptive filter tap weights by jointly minimizing ~~the~~ a cost function between the received signal and ~~the~~ a sum of ~~the~~ outputs of the respread processors of previous SIC-ATRF processors; and

updating, in the ATRF, the filter tap weights.

Claim 18 (original): The method of claim 17 wherein the pre-determined cost function is a minimum mean square error function.

Claim 19 (currently amended): A method in a combination system for enabling ~~the~~ a receiver to receive ~~input~~ user signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering the user signals according to a pre-defined methodology and assigning each user signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, a frequency shift processor, an adaptive temporal ~~filter;~~ filter, and a complex mathematical operation processor for canceling ~~the~~ a reconstructed signal ~~for the user~~ from ~~the total~~ a received ~~signal.~~ signal;

communicating a separate user code associated with the user signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

shifting, in the frequency shift processor, the symbol estimate generated by the respread processor for the user signal associated with the SIC-ATRF processor;

estimating a channel for the user signal associated with the SIC-ATRF processor and reconstructing ~~the~~ a signal interference associated with the user signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the user signal associated with the SIC-ATRF processor from the ~~total~~ received ~~signal.~~ signal to create an output; and

~~If~~ if a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to ~~the~~ a next successive SIC-ATRF processor.

Claim 20 (currently amended): The method of claim 19 wherein the channel estimation step further comprises:

determining ~~the~~ adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

Claim 21 (currently amended): The method of claim 19 wherein the channel estimation step further comprises:

determining ~~the~~ adaptive filter tap weights by jointly minimizing ~~the~~ a cost function between the received frequency shift estimate and ~~the~~ a sum of ~~the~~ outputs of the frequency shift processors of previous SIC-ATRF processors; and

updating, in the ATRF, the filter tap weights.

Claim 22-53 (cancelled)

Claim 54 (currently amended): In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive ~~input~~ user signals at varied power levels in the presence of interference wherein ~~said~~ an input signal to said receiver is a vector comprised of one signal from each antenna in an antenna array of the receiver, said combination comprising:

a control processor comprising a means for ordering user signals; and

a plurality of STAP/VSIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection, space-time adaptive processing and adaptive temporal reconstruction filtering in a successive arrangement wherein ~~the~~ an output of one of ~~the~~ said processors is ~~the~~ a vector input to ~~the~~ a next successive processor, each of said STAP/VSIC-ATRF processors comprising:

a space-time adaptive processing (STAP) processor;

a plurality of adaptive temporal filters (ATRFs), one per antenna; and

a plurality of complex mathematical operation processors, one per ATRF, for canceling ~~the~~ a reconstructed signal ~~for the user~~ from the ~~total~~ received input signal.

Claim 55 (original): The combination of claim 54 wherein each STAP processor comprises:

a plurality of filters, one per antenna;

a mathematical summation processor for combining the outputs of all the filters;

a conventional detector; and

a minimum cost channel weight update processor.

Claim 56 (original): The combination of claim 55 wherein the STAP processor is a blind adaptive STAP processor.

Claim 57 (original): The combination of claim 55 wherein each STAP/VSIC-ATRF processor further comprises a plurality of respread processors.

Claim 58 (original): The combination of claim 55 wherein each STAP processor further comprises a respread processor.

Claim 59 (original): The combination of claim 54 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

Claim 60 (original): The combination of claim 59 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

Claim 61 (currently amended): The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, ~~the~~ an output of the respread processor is ~~the~~ an input for the plurality of ATRFs.

Claim 62 (currently amended): The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, ~~the~~ an input to the plurality of ATRFs further comprises ~~the~~ outputs of the respread processors in all the previous STAP/VSIC-ATRF processors.

Claim 63 (original): The combination of claim 57 wherein each STAP/VSIC-ATRF processor further comprises a plurality of frequency shift processors connected between the respread processor and the plurality of ATRFs.

Claim 64-75 (cancelled)